

AMENDED CLAIMS WITHOUT SHOWING CHANGES MADE

- Board Decision*  
*F1*
1. A method of forming a semiconductor device, comprising:  
forming a first interconnect level over a semiconductor substrate;  
forming an uppermost interconnect level that includes an interconnect portion and a bond pad over the first interconnect level, wherein:  
the interconnect portion contacts the first interconnect level by way of vias through an interlevel dielectric layer, and wherein all vias interconnecting the interconnect portion and the first interconnect level are positioned outside regions directly below the bond pad;  
forming a passivation layer over the uppermost interconnect level;  
removing portions of the passivation layer, wherein removing portions of the passivation layer exposes portions of the bond pad and forms a plurality of support structures overlying the uppermost surface of the bond pad; and  
forming a conductive capping layer overlying the plurality of support structures, wherein the conductive capping layer electrically contacts the bond pad.

- F2*
8. The method of claim 1, further comprising forming a barrier layer between the capping layer and the bond pad, wherein the barrier layer overlies the support structures and abuts exposed portions of the bond pad.

- Board Decision*  
*F3*
24. A method of forming a semiconductor device, comprising:  
depositing a dielectric layer over a semiconductor substrate;  
patterning and etching a trench opening within the dielectric layer;  
depositing a copper layer over the dielectric layer and within the trench opening;

*Fig 3*  
*mul*

removing portions of the copper layer not contained within the trench opening to define an uppermost interconnect level comprising a copper bond pad and an interconnect portion, wherein the interconnect portion physically couples to an underlying interconnect level by way of vias, wherein the vias are positioned beyond regions directly below the copper bond pad;  
forming a passivation layer over the uppermost copper bond pad;  
patterning and etching the passivation layer to define openings and support structures overlying the uppermost copper bond pad;  
depositing a conductive layer over the support structures and within the openings, wherein the conductive layer electrically contacts the uppermost copper bond pad;  
patterning and etching the conductive layer to define a capping film over the support structures and the openings.

---

- Board Decision*
- Fig 4*
32. A method of forming a semiconductor device, comprising:  
forming an uppermost interconnect level over a semiconductor substrate, wherein the uppermost interconnect level includes an interconnect portion and a bond pad, wherein the bond pad has dielectric studs disposed within the bond pad;  
forming a passivation layer over the uppermost interconnect level;  
removing portions of the passivation layer, wherein removing portions of the passivation layer exposes portions of the bond pad and forms a plurality of support structures overlying the uppermost surface of the bond pad, wherein at least a portion of a support structure overlies a portion of a dielectric stud; and